REMARKS

At the outset, Applicant appreciates the thorough review and consideration of the subject application. The Non-Final Office Action of April 28, 2004, has been received and its contents carefully noted. Claims 1-29 are currently pending. By this amendment, claims 1-11 and 16 are amended and claims 21-29 are newly added. Support for these amendments are provided in at least Figures 1-3 and related text of the specification. No new matter has been added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,229,513 issued to Nakano, *et al.* ("Nakano") in view of U.S. Patent No. 6,356,260 issued to Montalbo, *et al.* ("6,356,260"). Applicant respectfully traverses this rejection for at least the following reasons.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation in the references themselves to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success for the modification or combination of references. Applicant respectfully submits that a *prima facie* case of obviousness has not been established.

Claim 1 recites, *inter alia,*

> a first connecting member having a data driver that converts the RSDS specification into TTL data that generates a column signal

> when the image data, the control signal, and the gray scale voltage are applied.

None of the applied references teach or suggest at least these features.

Nakano is directed towards an LCD apparatus having a display control unit for lowering clock frequency at which pixel drivers are driven. In Nakano, a data bus line transmits originally ordered display data from the computer side to drain drivers. *See* col. 4, ll. 38-41. More specifically, the drain driver does not receive the LVDS signal or convert the LVDS signal. In contrast, the invention of claim 1 transmits an encoded image and the control signal of the RSDS specification from the system to the first connecting member through the control board. This is simply not taught by Nakano. Also, Nakano fails to teach an encoder disposed in the system. The Examiner admits Nakano is materially deficient and tries to cure the deficiencies of Nakano with Montalbo.

Montalbo discloses RSDS data generated in the flat panel display system. *See* Figs. 3C, 5, col. 7, ll. 19. In contrast, the encoder of claim 1 is arranged in the system. More specifically, claim 1 recites a system,

> including an image processing part that decides for deciding a timing format of an image data and generating a control signal for the image data, an encoder for encoding the image data and the control signal output from the image processing part into a RSDS specification, and a power output part that outputs for outputting a constant-voltage.

This is simply not taught by the applied references. The system corresponds to the host computer of the applied references. In the present invention of claim 1 it is unnecessary to mount elements for encoding and decoding data and control signal on the control board and to design the elements, and the mounting area of the control board is minimized and the structure of the circuit of the control board is simplified.

Claim 6 recites, *inter alia,*

> a signal converting board including an analog/digital converter that converts an analog data having an analog format and forms a picture and a control signal for the analog data into a digital data and a digital control signal, an image processing part that decides a timing format of the digital data and generates a control signal for the digital data, and an encoder that encodes the digital data and the digital control signal output from the image processing part into encoded digital data and encoded digital control signal having a RSDS specification.

Claim 11 recites, *inter alia,*

> a system including a image signal processing part, a power output part, and encoder part, wherein the image signal processing part generates a data signal and a control signal and the encoder part receives the data signal and the control signal and transmits RSDS signals.

For similar reasons as discussed above none of the applied references teach or suggest at least these features. More specifically, Montalbo discloses RSDS data generated in the flat panel display system. *See* Figs. 3C, 5, col. 7, ll. 19. In contrast, the encoder part of claim 11 is arranged in the system and the encoder of claim 6 is arranged in the signal converting board. These limitations are not taught or suggested by the applied references.

Accordingly, Applicants respectfully submit a prima facie case of obviousness has not been established and request withdrawal of the rejection under 35 U.S.C. § 103.

Added Claims

Added claims 21-29 are directed to additional aspects of the invention, which are not disclosed or suggested in the art of record.

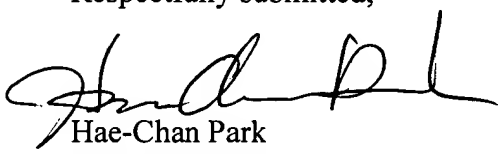
CONCLUSION

Applicant believes that a full and complete response has been made to the pending Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicant respectfully submits that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant's undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,



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